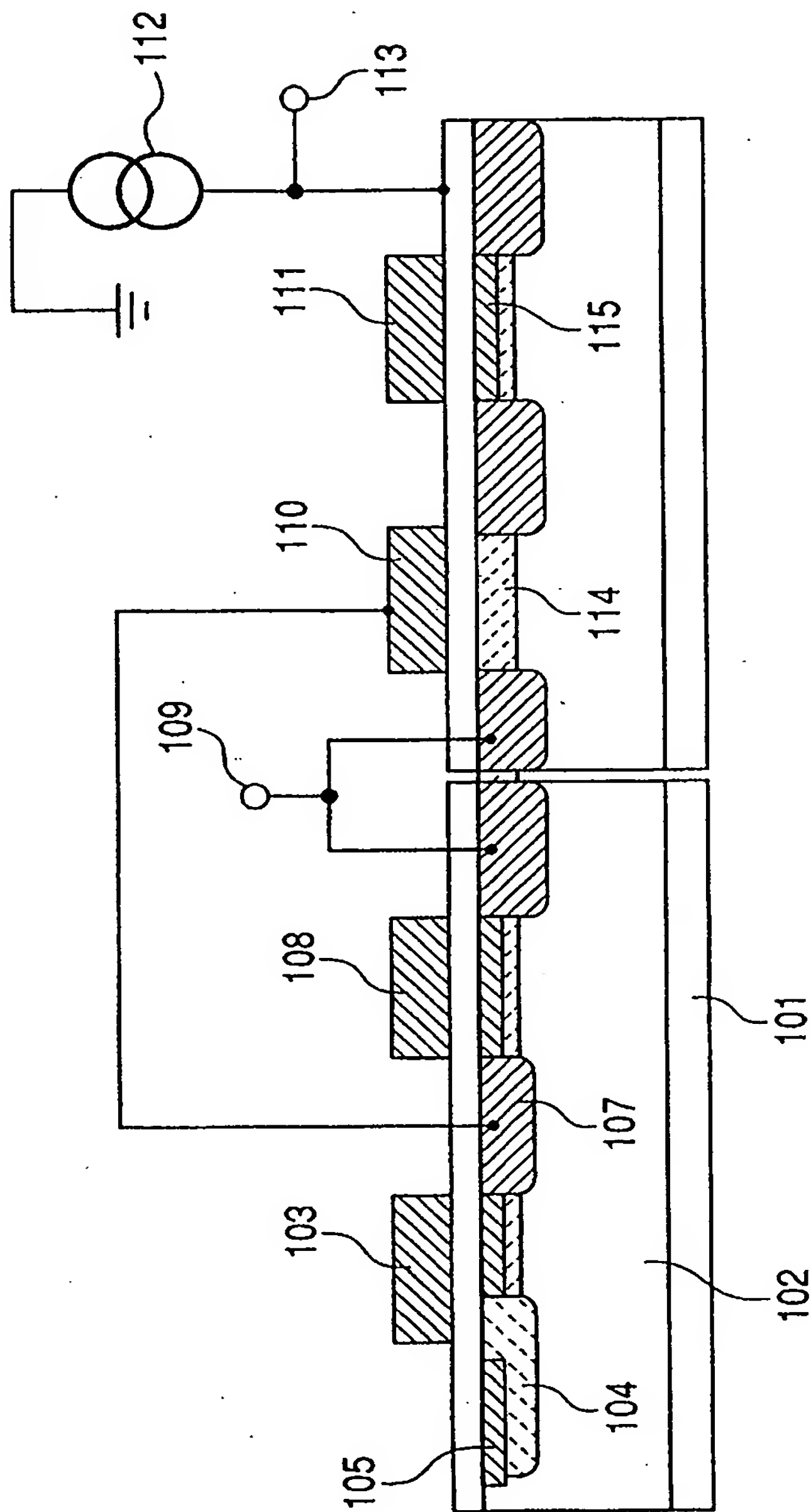


1 / 9

FIG. 1



2 / 9

FIG. 2A

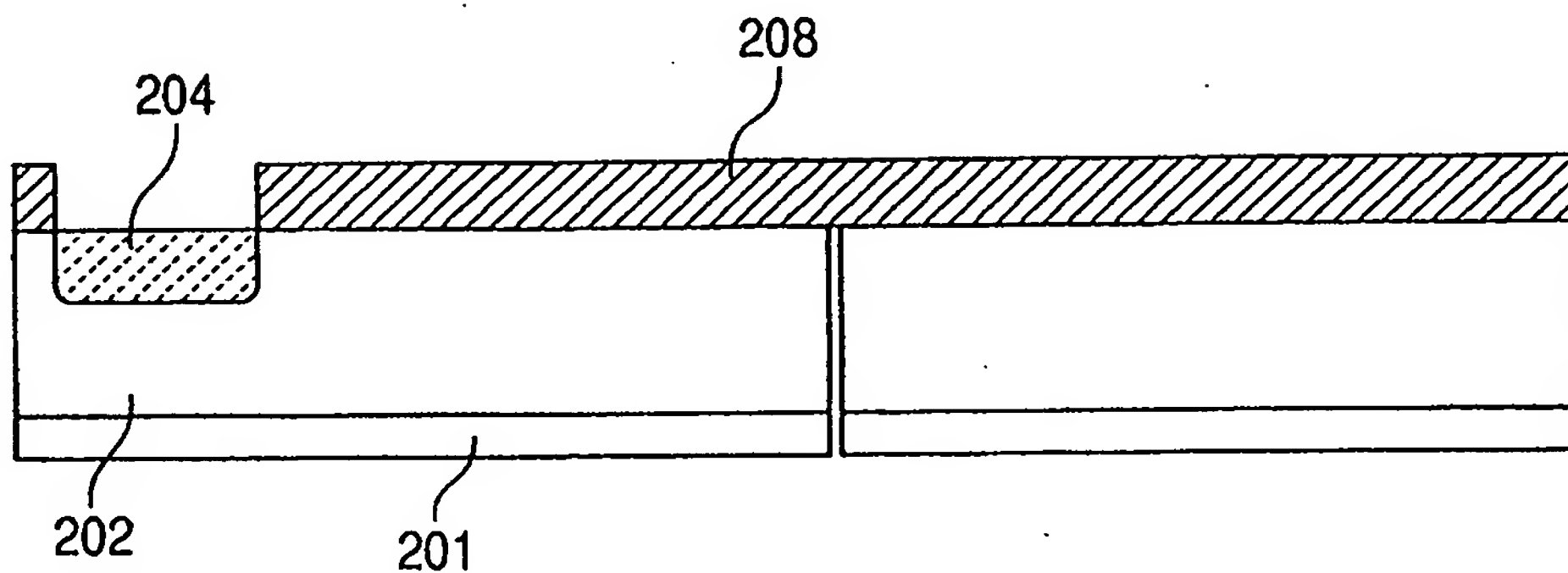


FIG. 2B

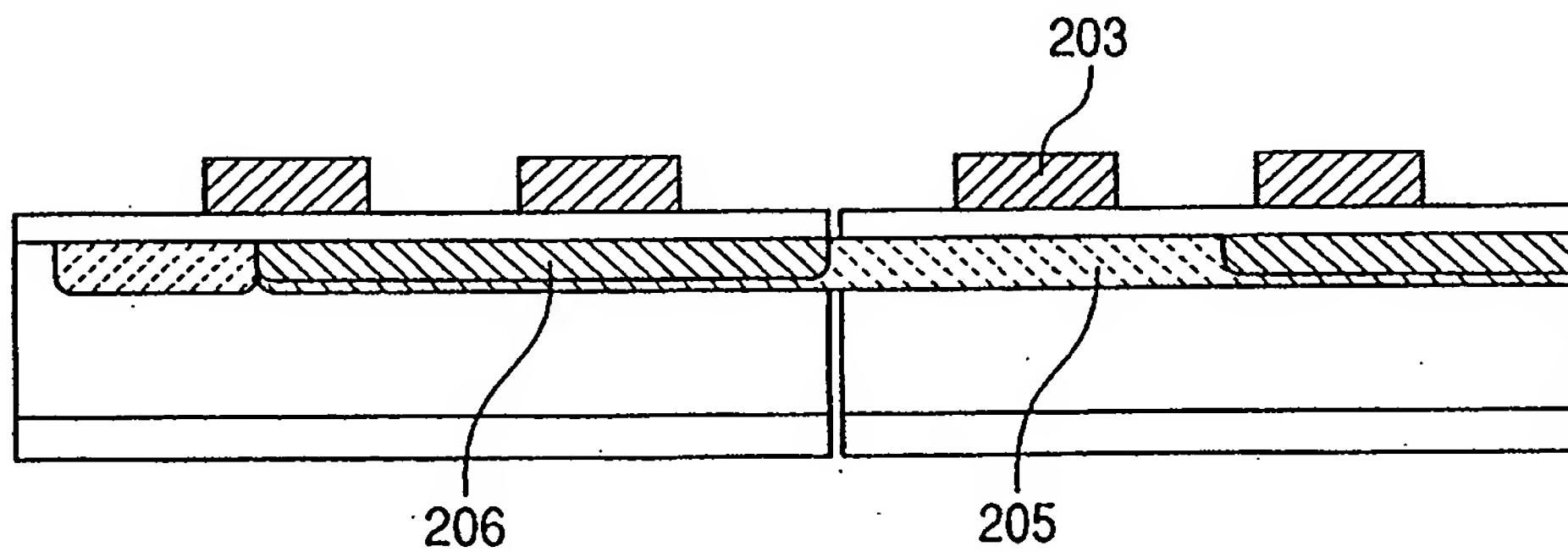
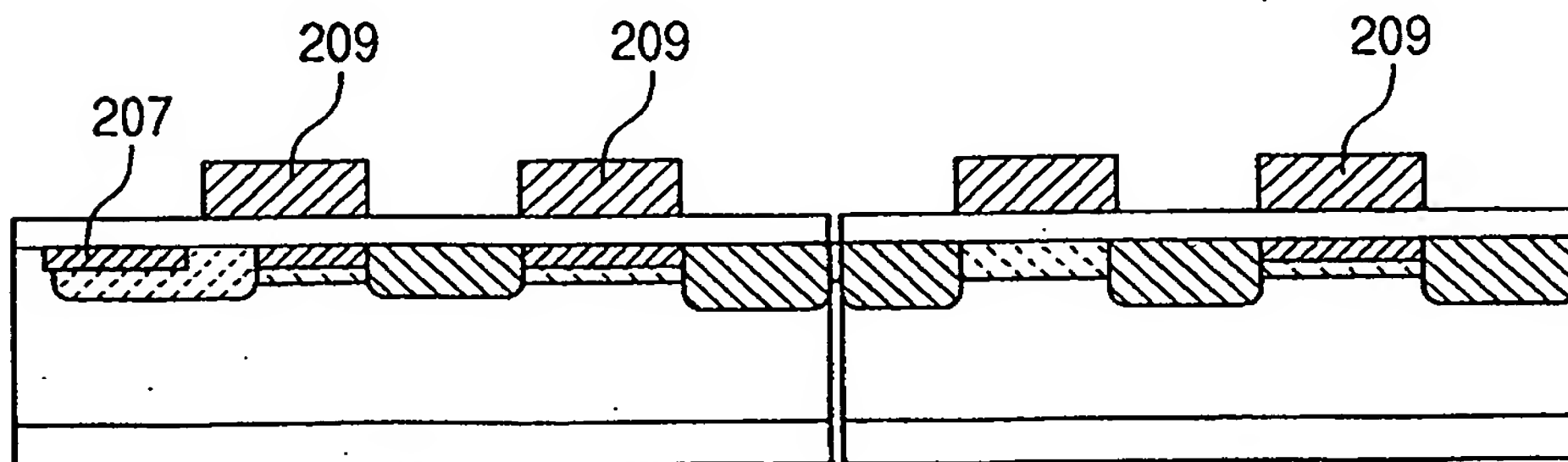
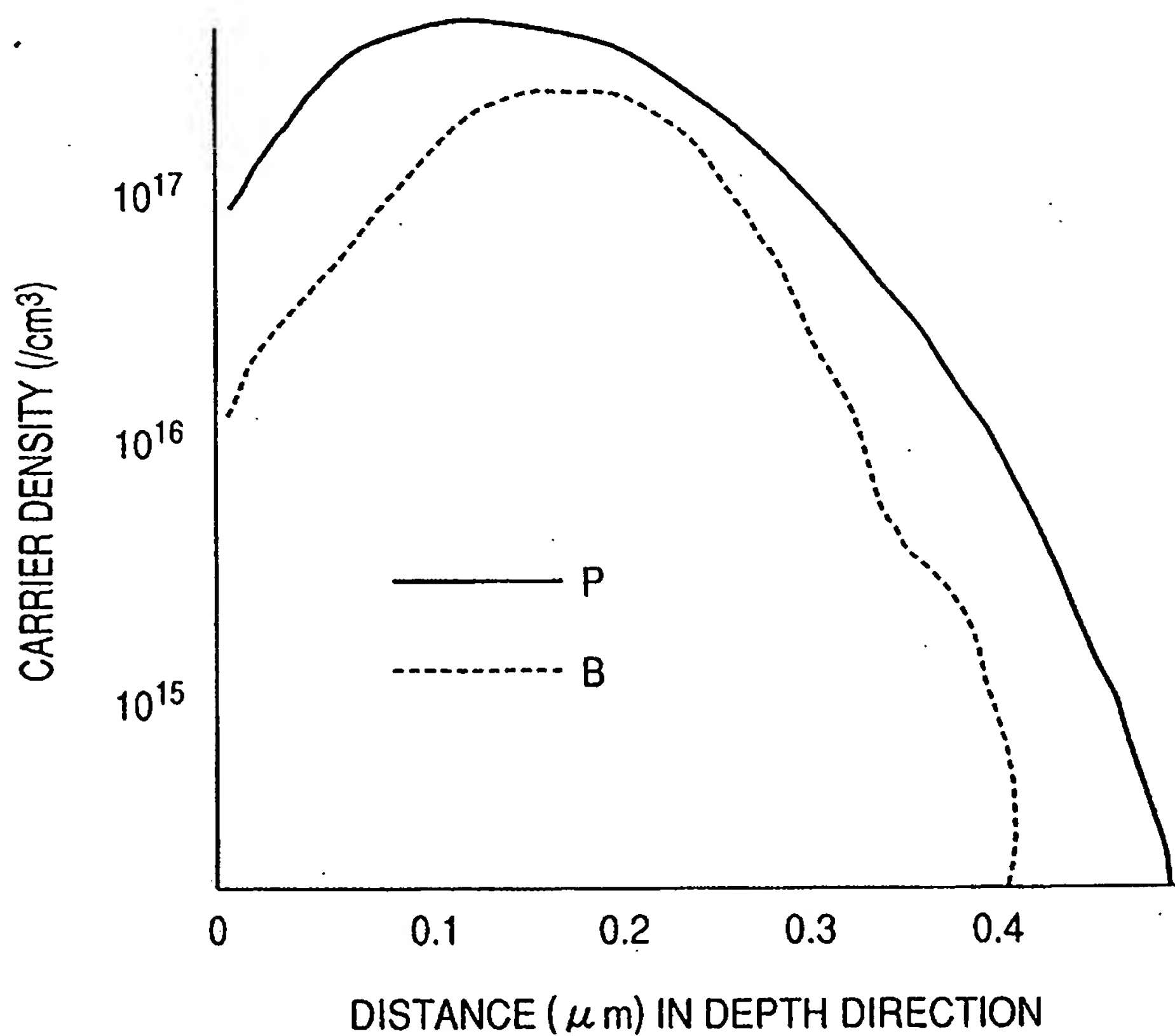


FIG. 2C



3/9

FIG. 3



4/9

FIG. 4A

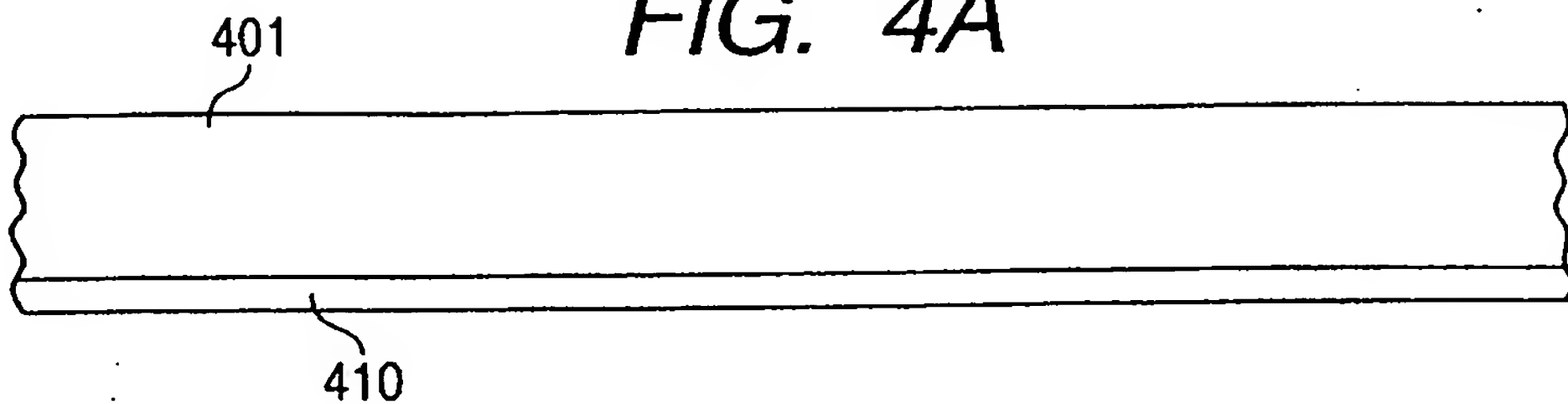


FIG. 4B

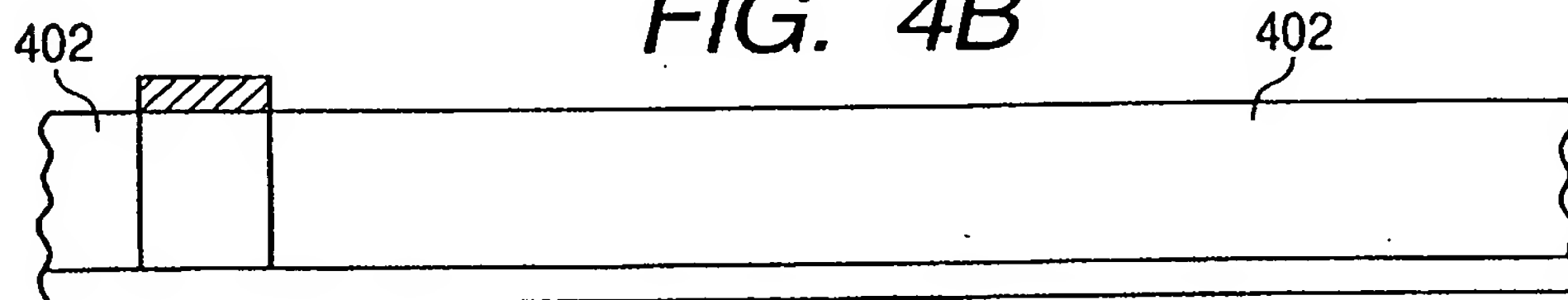


FIG. 4C

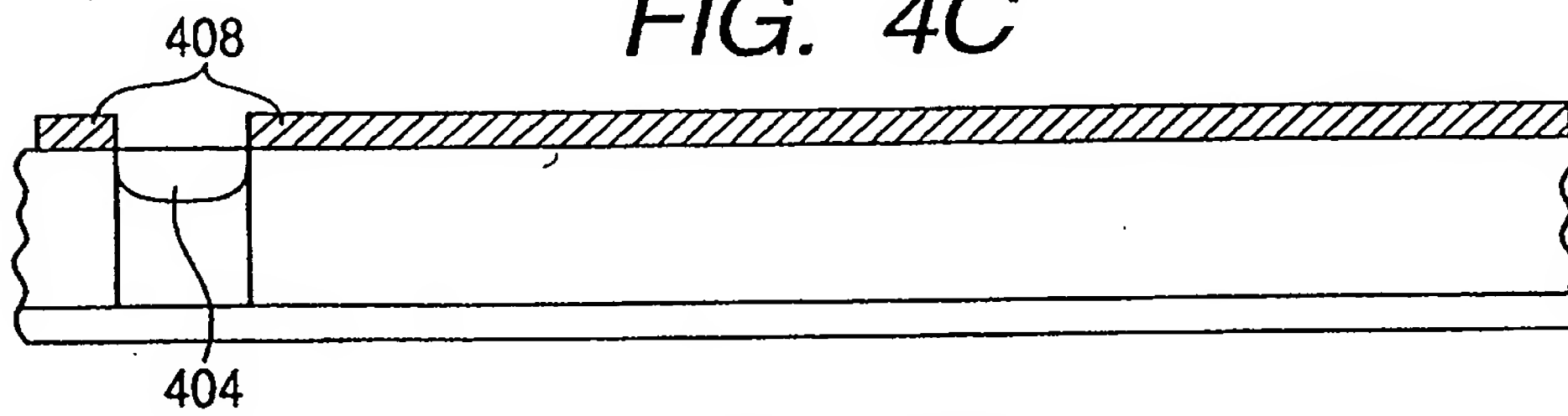


FIG. 4D

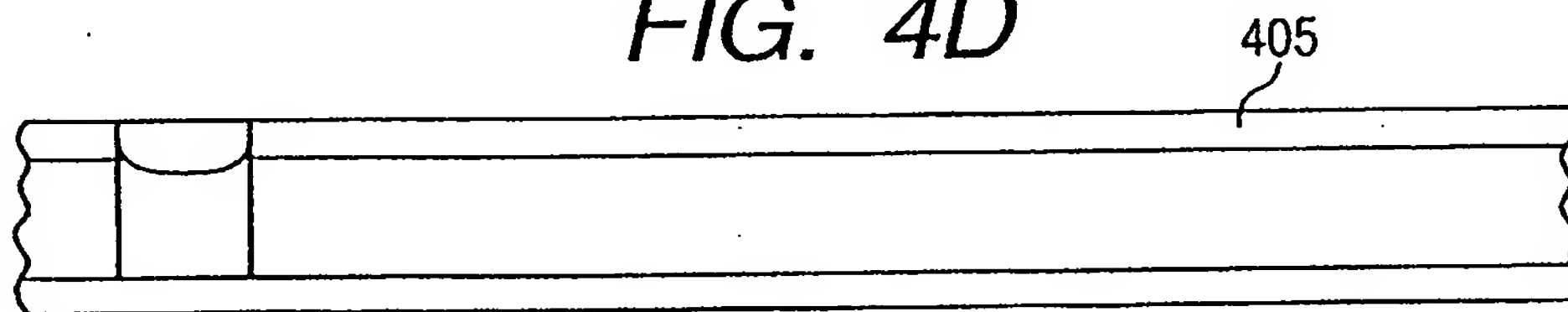


FIG. 4E

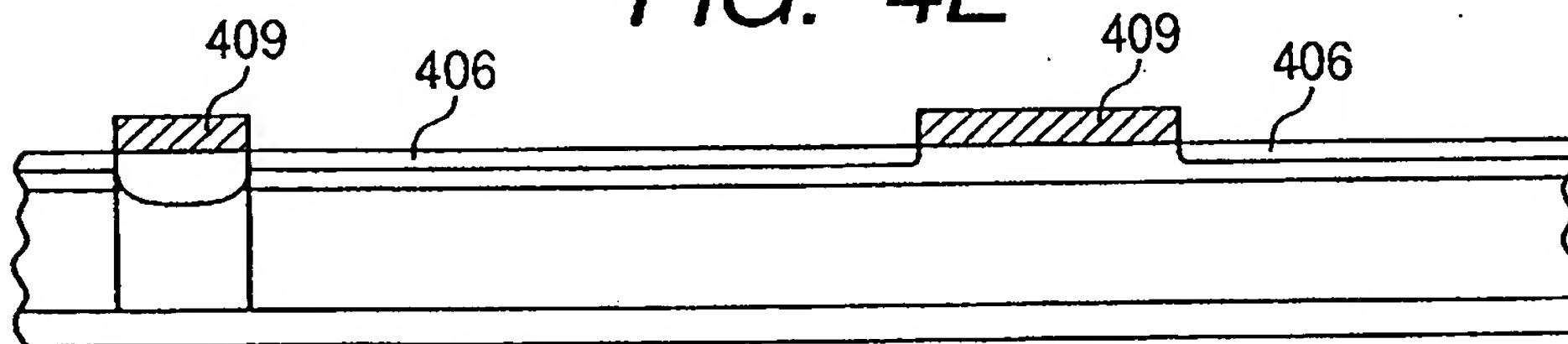
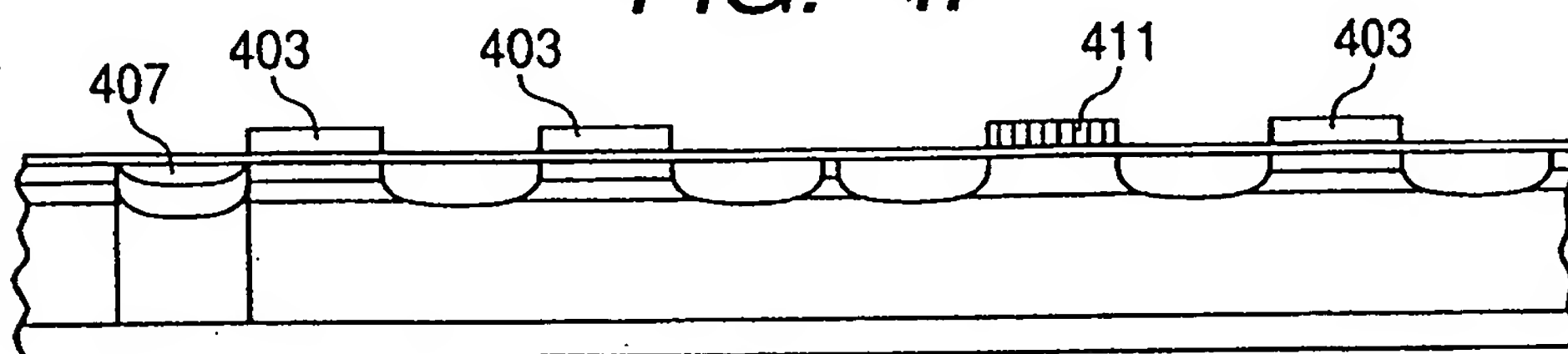
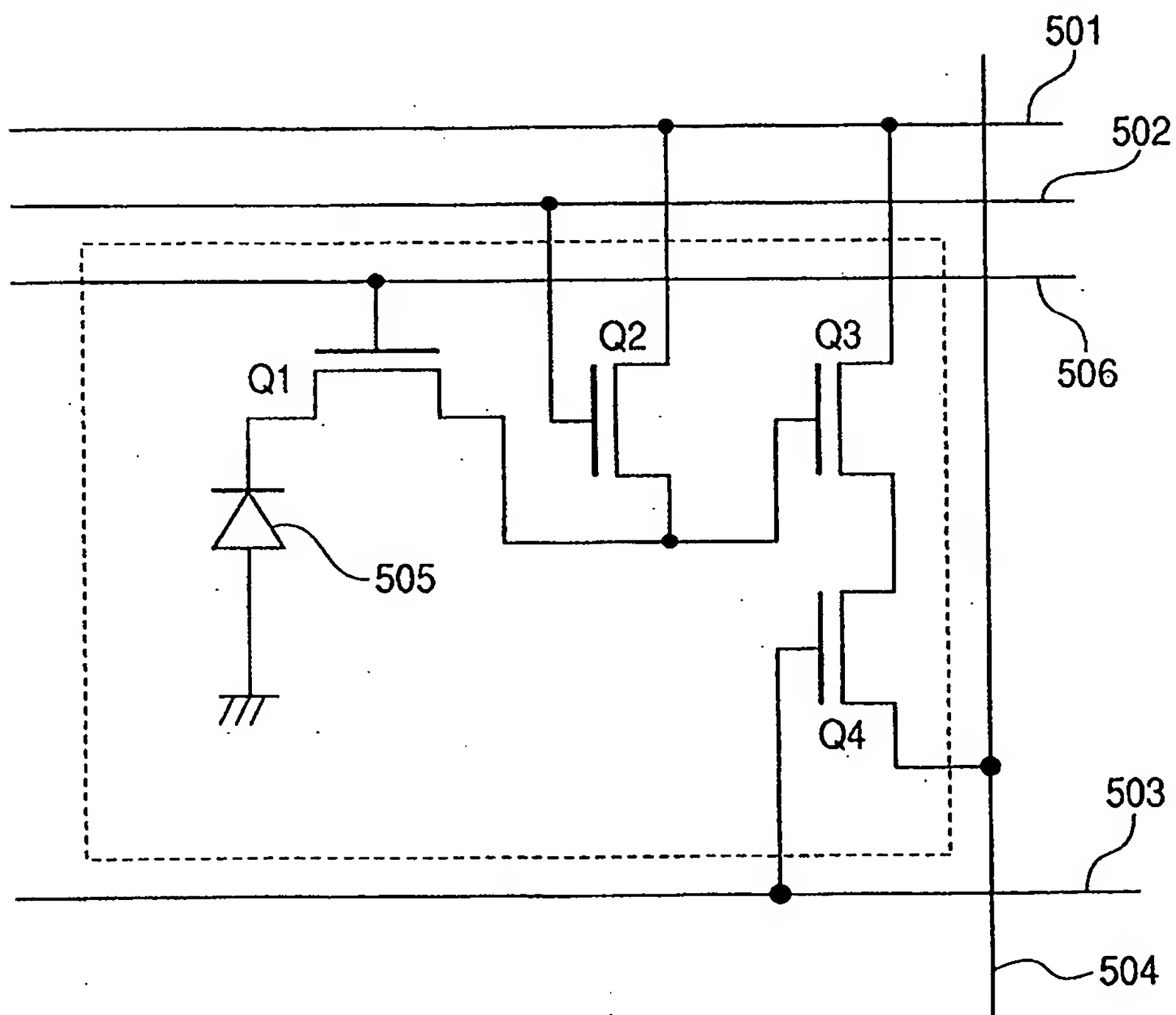


FIG. 4F



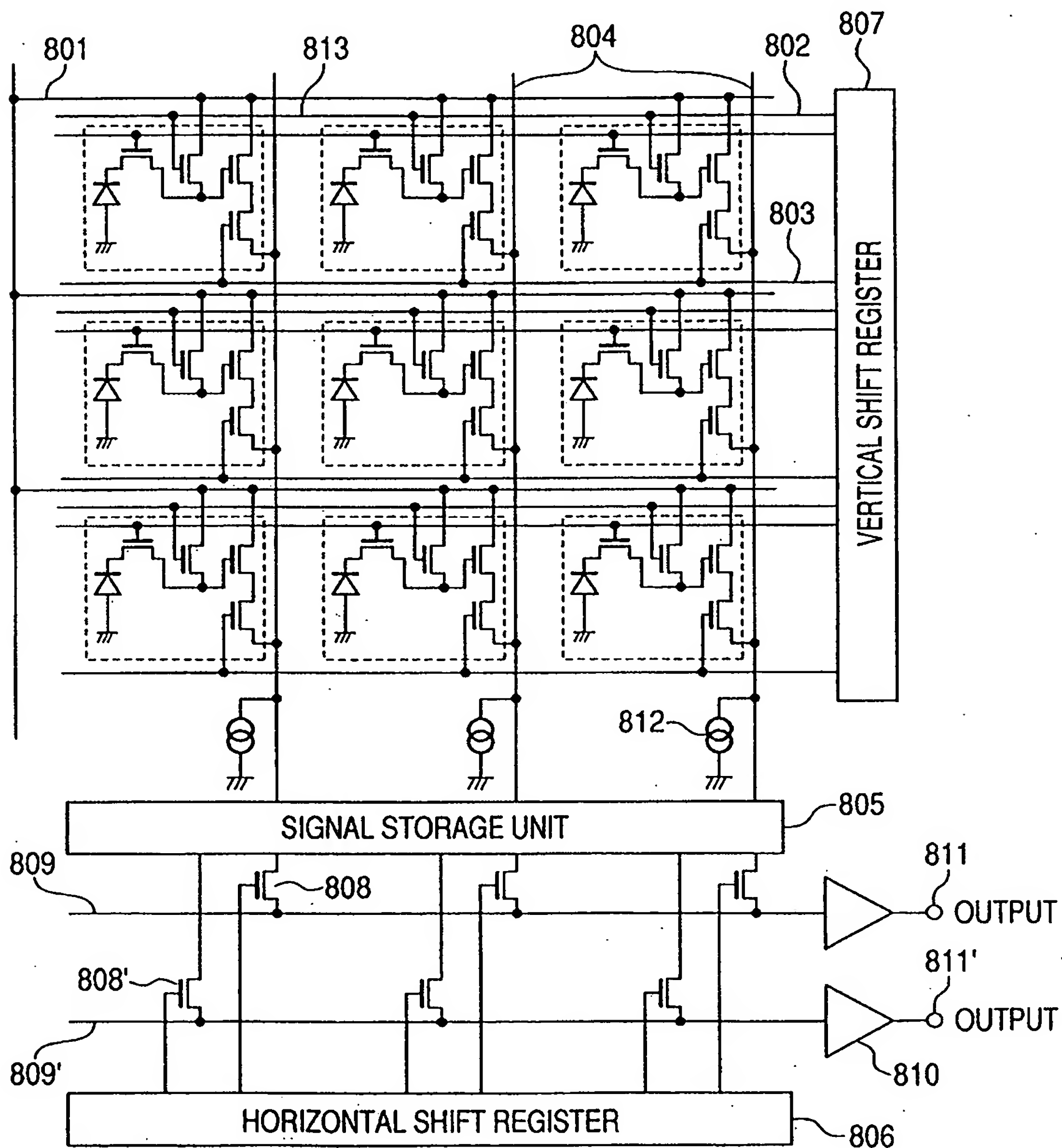
5/9

FIG. 5



6 / 9

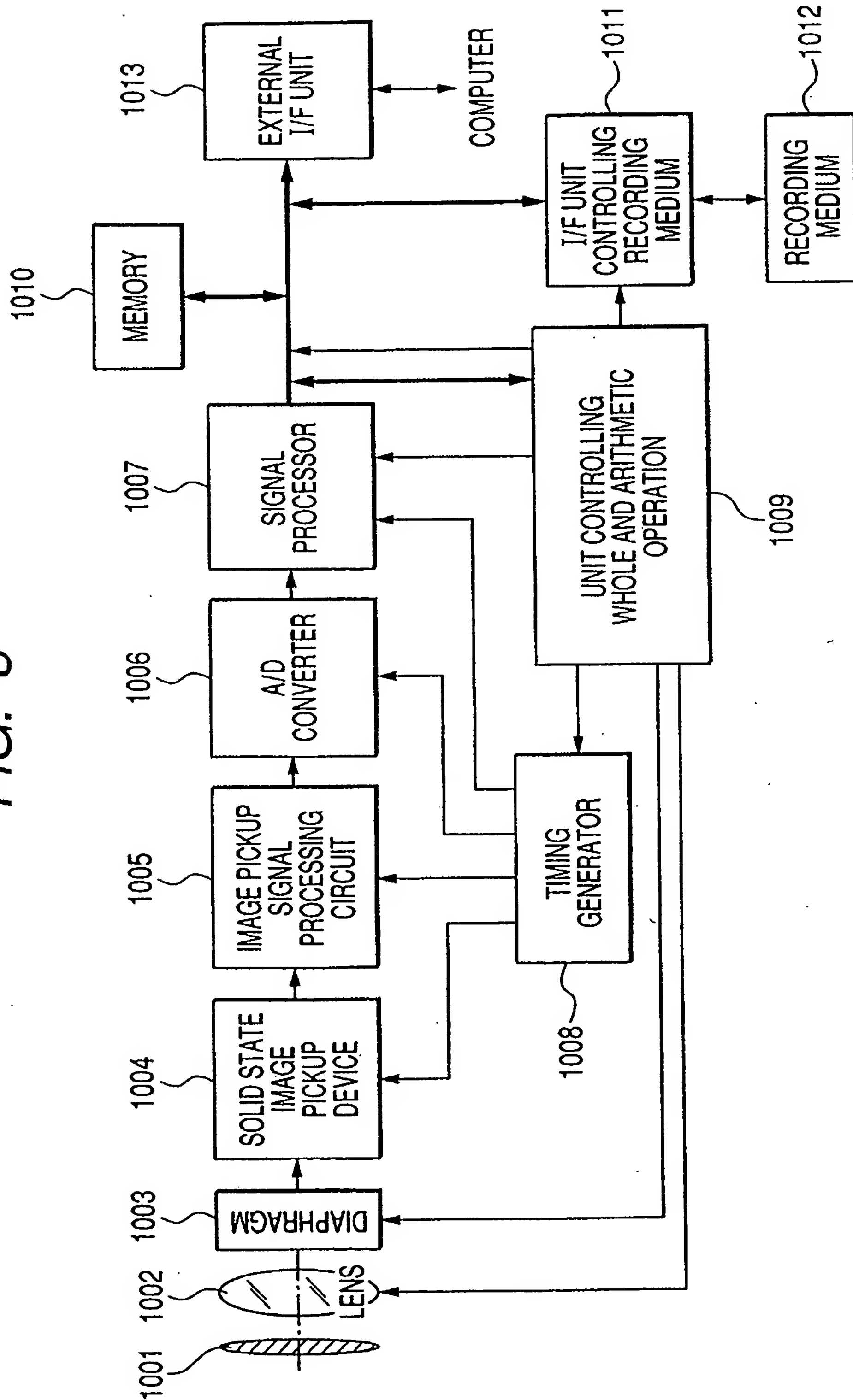
FIG. 6



This cross-sectional view shows a semiconductor device with a multi-layered structure. At the bottom is a substrate 901. Above it is a layer 902. A thick layer 906 is formed on top of 902. On the surface of 906, there are several rectangular regions 907, each containing a small circular feature. To the left of these regions is a series of rectangular blocks 903. Above the 906 layer is a thin layer 908. Above 908 is a layer 914, which contains circular features 909 and 910. The entire structure is capped by a top layer 904. Electrical connections are shown on the left, with labels $\phi 1$ and $\phi 2$ indicating different potential levels or contacts.

8 / 9

FIG. 8



9/9

FIG. 9A

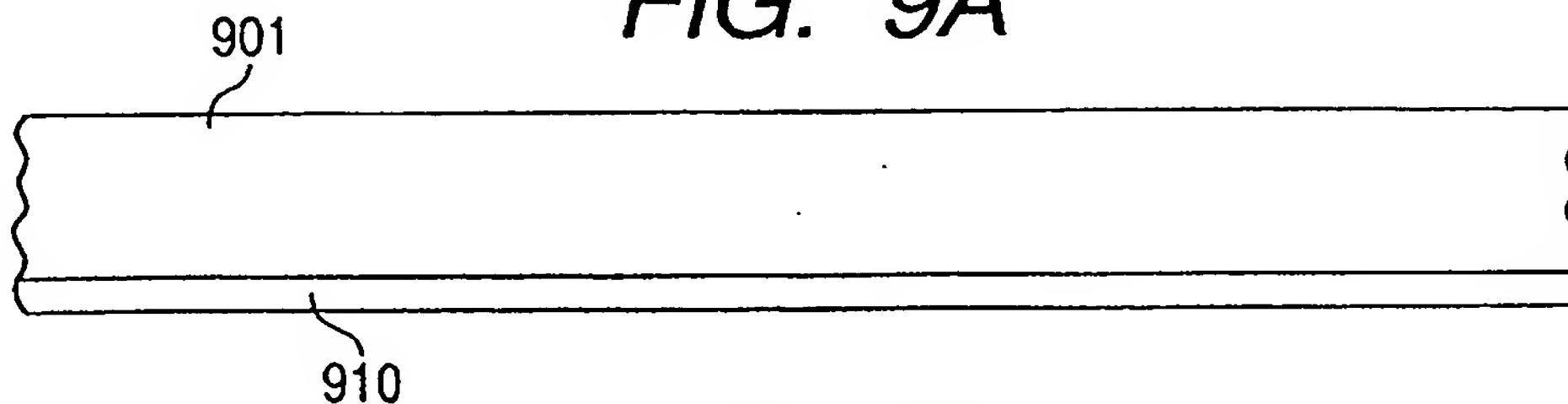


FIG. 9B

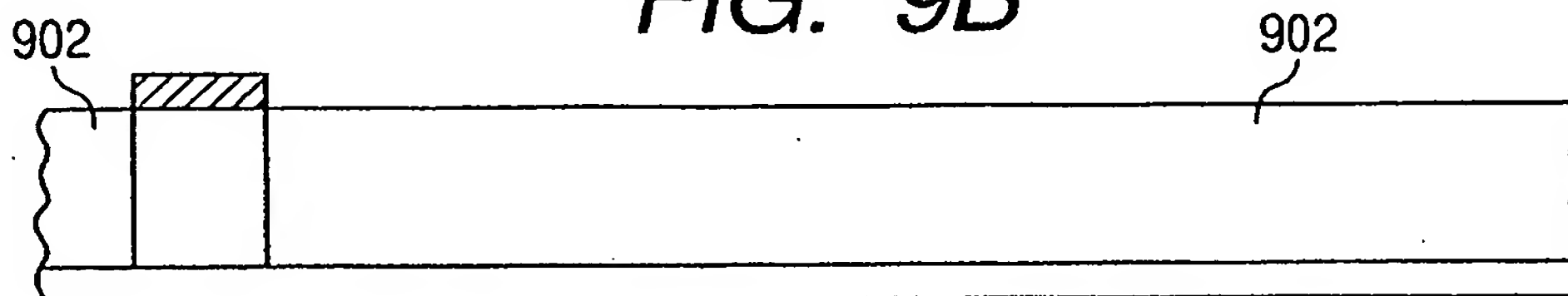


FIG. 9C

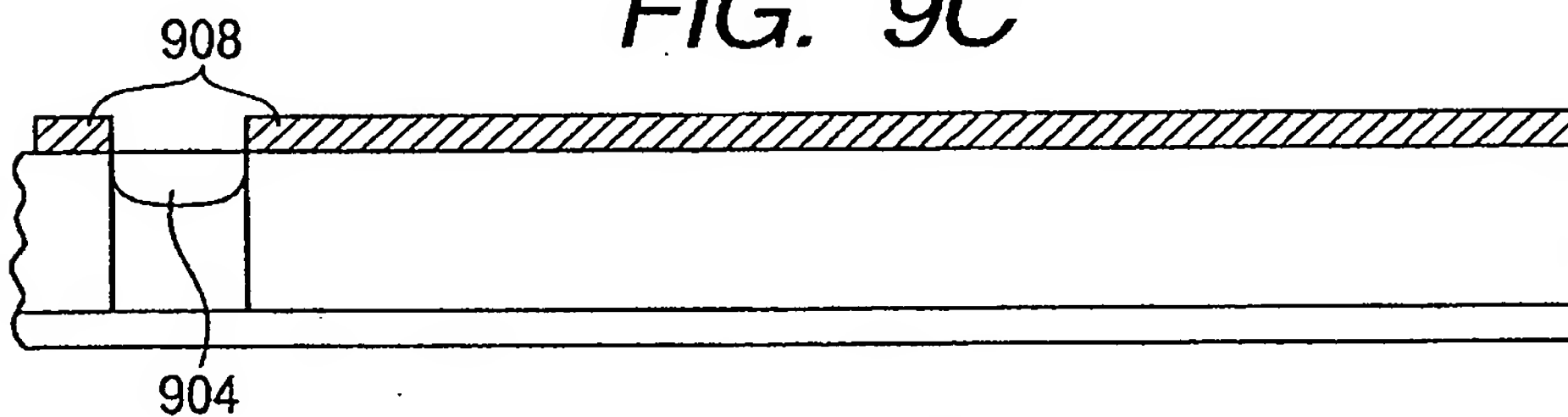


FIG. 9D

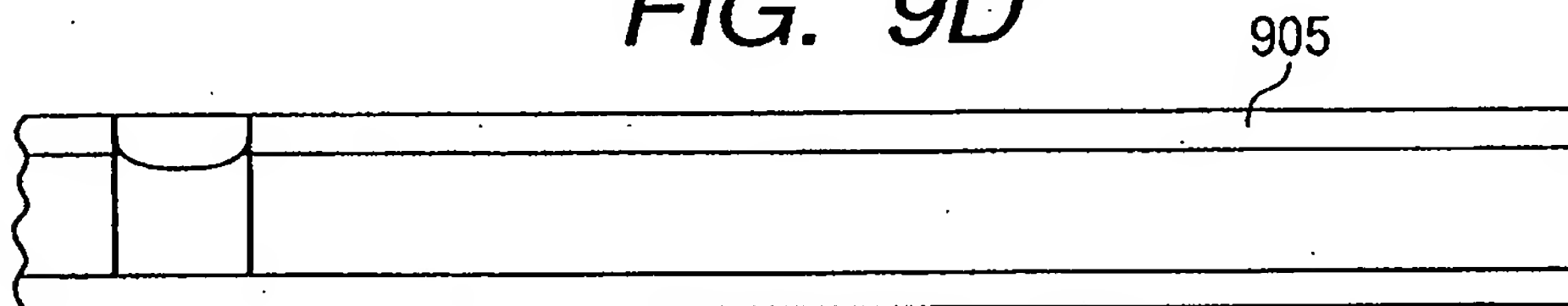


FIG. 9E

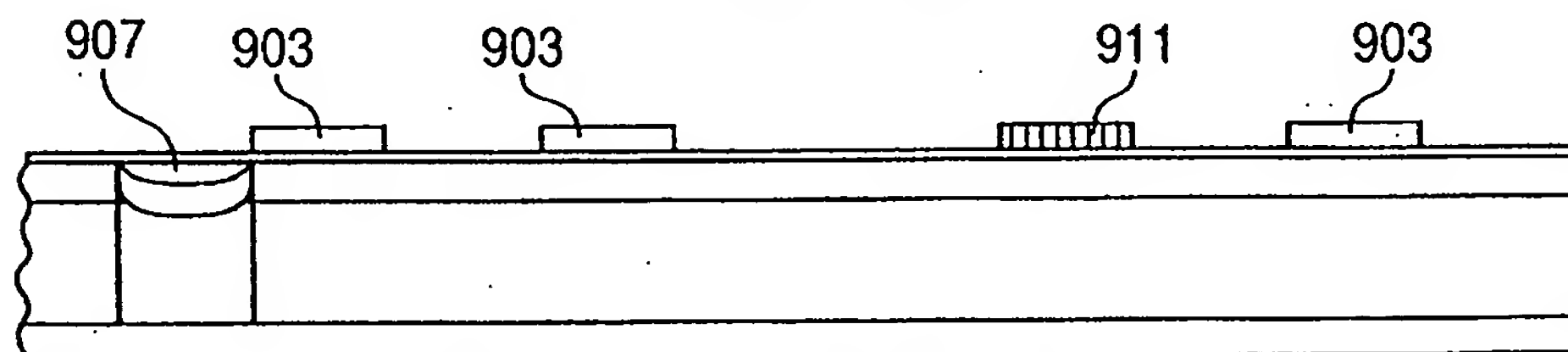


FIG. 9F

